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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/517,804	03/02/2000	Amit Gulati	9804-015-999	4426

33438 7590 08/20/2004

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EXAMINER	
WONG, ALLEN C	

ART UNIT	PAPER NUMBER
2613	14

DATE MAILED: 08/20/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/517,804	GULATI ET AL.	
	Examiner	Art Unit	
	Allen Wong	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9,13,14 and 16-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9,13,14 and 16-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 5/26/04 have been fully read and considered but they are not persuasive.

Regarding lines 15-17 on page 5 of applicant's remarks about claims 1 and 13, applicant asserts that Cheney does not disclose the word "cache" or anything equivalent. The examiner respectfully disagrees. Cheney's fig.4, element 402 is an instruction storage that can similarly function like a cache where element 402 processes video data stream instructions and interactively functions with other elements of fig.4 such as decode subsystem 301, controller 401, etc. Thus, Cheney discloses the *cache memory* 402 *is distinct* from the *scalable buffer* 601.

Regarding lines 21-24 on page 5 of applicant's remarks about claims 1 and 13, applicant mentions that Cheney does not teach the determination of the optimal buffer size and the scalable buffer. The examiner respectfully disagrees. In col.12, lines 13-45, fig.4, element 401 is the controller module or analysis module that is interactive with all parameters presented to element 401 for analysis. Cheney teaches the adjustment of a buffer size register and a spill size register for minimizing memory use and permit efficient decoding, and that since the elements function interactively together, there is a relationship between the buffers, as disclosed col.14, lines 25-36. In fig.4, Cheney's element 600 is a buffer management module that appropriates the first and second buffer sizes for scalable buffer 601 so as to appropriately store data with the right amount of

space required for efficient memory management. Thus, Cheney teaches the determination of the optimal buffer size and the scalable buffer.

Regarding lines 14-20 on page 6 of applicant remarks about claims 1 and 13, applicant states that Smith does not teach a method of determining an optimum buffer size for a scalable buffer in the main memory based upon the correspond cache memory performance. The examiner respectfully disagrees. The examiner has already mentioned reasons that the determination of the scalable buffer's optimum buffer size in the above paragraphs and in the rejection below.

Also, Smith is relevant to the discussion to this case because it discloses the improving the allocation of memory and cache to minimize false cache reads and inaccurate storage and retrieval of data, as stated in col.3, lines 41-48. Smith is cited because Cheney fails to disclose the limitation of wherein the memory utilization data that includes cache miss rate data. Therefore, it would have been obvious to one of ordinary skill in the art to take the teachings of Cheney and Smith, as a whole, for utilizing the memory utilization data that includes the cache miss rate data so as to enhance, improve the cache memory performance. Doing so would speed the task of decoding high quality images for viewing and save costs in the long run with smooth, efficient memory performance routines.

Regarding lines 27-28 on page 6 of applicant's remarks, applicant argues that Cheney does not disclose the storage of video data stream processing instructions. The examiner respectfully disagrees. Cheney's fig.4, element 402

is an instruction storage that can similarly function like a cache where element 402 processes video data stream instructions and interactively functions with other elements of fig.4 such as decode subsystem 301, controller 401, etc. Thus, Cheney discloses the *cache memory* 402 *is distinct* from the *scalable buffer* 601.

Claims 2-9 and 14, 16-22 are rejected for the same reasons as independent claims 1 and 13.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-9, 13-14, 16-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney (5,668,599) in view of Smith (5,802,600).

Regarding claim 13, Cheney discloses a computer readable memory to direct a computer to function in a specified manner, comprising:

a buffer management module to establish a first buffer size and a second buffer size for a scalable buffer (fig.4, element 600 is a buffer management module that appropriates the first and second buffer sizes for scalable buffer 601);

a video decoding module to process a video stream with said scalable buffer configured to said first buffer size and said second size (fig.4, element 301); and

an analysis module to create memory utilization data characterizing cache memory performance during the processing with said scalable buffer configured to said first buffer size and during the processing with said scalable buffer configured to said second buffer size, said analysis module including a buffer size adjuster to assign a buffer size that is dependent upon said first buffer size and said second buffer size for said scalable buffer in accordance with said memory utilization data (col.12, lines 13-45, fig.4, element 401 is the controller module or analysis module that is interactive with all parameters presented element 401 for analysis; further, Cheney teaches the adjustment of a buffer size register and a spill size register for minimizing memory use and permit efficient decoding, and that since the elements function interactively together, there is a relationship between the buffers, as disclosed col.14, lines 25-36), and

the cache memory is distinct from the scalable buffer (in fig.4, element 402 is an instruction storage that can similarly function like a cache where element 402 processes video data stream instructions and interactively functions with other elements of fig.4 such as decode subsystem 301, controller 401, etc., thus the *cache memory* 402 *is distinct* from the *scalable buffer* 601).

Although Cheney does not specifically disclose the limitation of wherein the memory utilization data that includes cache miss rate data. However, Smith teach the limitation of wherein the memory utilization data that includes cache

miss rate data (col.4, ln.1-12; Smith discloses that a cache allocation procedure can be implemented to reduce the cache miss rate by maintaining a record of the cache misses that occur in the cache memory portions, and then this record of cache misses, ie. memory utilization data, is utilized for adjusting, controlling or modifying the sizes of the cache memory portions, thus, the Smith teaches the relationship between the first and second memory portions as well as obtaining the cache miss rates data). Therefore, it would have been obvious to one of ordinary skill in the art to take the teachings of Cheney and Smith, as a whole, for utilizing the memory utilization data that includes the cache miss rate data so as to enhance, improve the cache memory performance. Doing so would speed the task of decoding high quality images for viewing and save costs in the long run with smooth, efficient memory performance routines.

Note claim 1 has similar corresponding elements.

Regarding claims 2, 14 and 15, Cheney discloses the definition of a buffer size as a multiple of an encoded image data block in the form of a macroblock (col.13, ln.45 to col.14, ln.3; Cheney discloses macroblock image formats 4:2:0 and 4:2:2, where a macroblock is a data unit that contains luminance and chrominance components, for instance, 4:2:0 chroma formatted macroblock comprises data covering a 16 pixel by 16 pixel section of the video frame and 4:2:2 chroma sampling format comprising four 8x8 blocks of luminance data and four corresponding 8x8 blocks of chrominance data).

Regarding claims 3 and 16, Cheney discloses the use of a variable length decoder (fig.4, element 311).

Regarding claims 4 and 17, Cheney discloses the use of an inverse discrete cosine transfer function (fig.4, element 331).

Regarding claims 5 and 18, Cheney discloses the use of a motion compensator (fig.4, element 341).

Regarding claims 8, 9, 21 and 22, Cheney discloses the adjustment of the buffer size (col.14, lines 25-36, Cheney teaches the adjustment of a buffer size register and a spill size register for minimizing memory use and permit efficient decoding).

If one is not convinced that Cheney discloses the buffer size adjustment, then one of ordinary skilled in the art can refer to the teachings of Smith to teach the adjustment of the buffer size (col.4, ln.1-12; Smith discloses the controlling, adjusting or modifying of the sizes of the first and second portions of the cache memory). Therefore, it would have been obvious to one of ordinary skill in the art to combine the teachings of Cheney and Smith, as a whole, for implementing the memory utilization data that includes the cache miss rate data so as to enhance, improve the cache memory performance. Doing so would speed the task of decoding high quality images for viewing and save costs in the long run with smooth, efficient memory performance routines.

Regarding claims 6, 7, 19 and 20, Cheney does not specifically disclose the use of cache miss rates. However, Smith teaches the use of cache miss rates (col.4, ln.1-12; Smith discloses that a cache allocation procedure can be implemented to reduce the cache miss rate by maintaining a record of the cache misses that occur in the cache memory portions). Therefore, it would have been

obvious to one of ordinary skill in the art to take the teachings of Cheney and Smith, as a whole, for implementing the memory utilization data that includes the cache miss rate data so as to enhance, improve the cache memory performance. Doing so would speed the task of decoding high quality images for viewing and save costs in the long run with smooth, efficient memory performance routines.

Conclusion

3. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Allen Wong whose telephone number is (703) 306-5978. The examiner can normally be reached on Mondays to Thursdays from 8am-6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Christopher Kelley can be reached on (703) 305-4856. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Allen Wong
Examiner
Art Unit 2613

AW
8/18/04

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